M.Sc. Thesis: VLSI architectures for Turbo Codes Adapted the Standard Mobile Communications WCDMA (3GPP TS 25.212)

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***Abstract*— Turbo Codes are a topic of great importance in communications systems. Therefore requires an analysis on architectures implemented so far. Simulations were performed in software of the turbo codes proposed by Berrou and established the 3GPP standard in order to monitor the performance of these varying different parameters. We carried out an analysis of the architecture and designs implemented so far and based on this we propose a new design with possible improvements in the design.**

I. Introduction

At present, the use of communication systems has grown in large quantities. For that reason requires communication systems make them more efficient data transmission, safe and with a better performance (faster transmission and more efficient use of bandwidth), in other words, communication systems more immune to noise and allowing transfers of large amounts of information. In 1948 Claude E. Shannon established the fundamental limits in transmission speeds in the systems of digital communications and led to the search for coding techniques for approaching the limit of this capacity [1].

The Turbo Codes are one of the most important developments in recent years within the channel coding, which are reaching the limits of the theoretical capacity of channel posed by C. E. Shannon. They were proposed by the French engineers Claude Berrou and Alain Glavieux in Geneva, Switzerland in 1993 [2,3].

Nowadays, the present standards of communications are incorporating turbo codes for the development of satellite links, in the space communication systems, the systems of third-generation telephony and also to increase the speed of data transmission in some versions of Wi-Fi networks.

There are many groups in the world researching and working on the issues and big companies such as Sony, NEC, Nokia, Motorola and chip and hardware manufacturers as Comtech AHA, Altera, Xilinx, among others.

In the country there is little development work on hardware implementation on turbo codes, which have an extensive field of research and applications. Some existing turbo codes implemented in hardware part of the intellectual property (IP) manufacturers, for example, Altera with "Turbo Encoder / Decoder MegaCore Function" implemented for the European standard WCDMA (3GPP TS 25,212) and Xilinx LogiCORE with, a turbo encoder and decoder for standard American CDMA2000 (TIA/EIA2002.2C).

II. Problem Definition

There are little architectures on turbo codes especially focused standard for mobile communications. Developments at the level of hardware that we find are available only as intellectual property of the manufacturers.

a. PROPOSAL

The proposed study, design and implementation reconfigurable hardware, the turbo decoding scheme defined in the specifications of the standard WCDMA (3GPP TS 25,212 V7.2.0).

b. GENERAL PURPOSE

Implementation material of a turbo decoder reconfigurable hardware (FPGA architectures, Field Programmable Gate Array) with the specifications of the European standard WCDMA (3GPP TS 25,212) [4].

c. PARTICULAR OBJETIVES

- Implement software scheme Turbo coding standard for WCDMA (3GPP TS 25,212).
- Design architecture of a turbo decoder.
- Developing a test bed.
- Validation of architecture.

In order to understand the operation of these, first we will see as it is its structure and operation.

III. Turbo Codes

TURBO ENCODER

The general structure used in turbo encoders is shown in Fig. 1. The turbo encoder is formed by the concatenation parallel of two encoders Recursive Systematic Convolutional, RSC separated by an interleaver (see Fig. 1). The interleaver [5] is a pseudo-random mixer block defined by a permutation of N elements without repeating any of them, in other words, adjusts the order of the sequence in a form giving a different order sequence with the original.

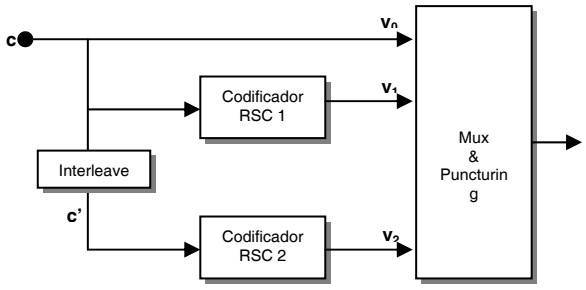

Figure 1. General structure of a turbo encoder.

Where the RSC encoder of 3GPP standard [4] has the following structure:

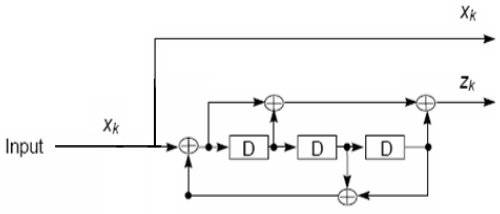

Figure 2. RSC encoder of 3GPP .

TURBO DECODER

The general structure of an iterative turbo decoder is shown in Figure 3. Two component SISO decoders are linked by interleavers and deinterleaver. As seen in the figure, each decoder takes three inputs: the systematically encoded channel output bits, the parity bits transmitted from the associated component encoder, and the information from the other component decoder about the likely values of the bits concerned. This information from the other decoder is referred to as a-priori information. The component decoders have to exploit both the inputs from the channel and this a-priori information. They must also provide what are known as soft outputs for the decoded bits. This means that as well as providing the decoded output bit sequence, the component decoders must also give the associated probabilities for each bit that has been correctly decoded. The soft outputs are typically represented in terms of the so-called Log Likelihood Ratios (LLRs). The polarity of the LLR determines the sign of the bit, while its amplitude quantifies the probability of a correct decision. Two suitable decoders are the Softh-Output Viterbi Algorithm (SOVA) y Maximun A Posteriori (MAP) Algorithm.

The decoder of Figure 3 operates iteratively, and in the first iteration the first component decoder takes channel output values only, and produces a soft output as its estimate of the data bits.

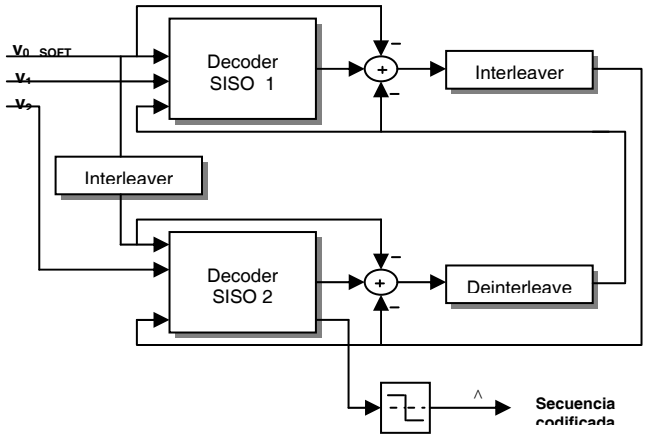

Figure 3. General structure of a turbo decoder

The soft output from the first encoder is then used as additional information for the second decoder, which uses this information along with the channel outputs to calculate its estimate of the data bits. Now the second iteration can begin, and the first decoder decodes the channel outputs again, but now with additional information about the value of the input bits provided by the output of the second decoder in the first iteration. This additional information allows the first decoder to obtain a more accurate set of soft outputs, which are then used by the second decoder as a-priori information. This cycle is repeated, and with every iteration the BER of the decoded bits tends to fall. However, the improvement in performance obtained with increasing numbers of iterations decreases as the number of iterations increases.

The algorithm MAP [6,7], we can see that it would be very difficult to implement in hardware for that reason there are modifications to this algorithm such as Log-MAP and MAP Max-Log, which are a logarithmic version of the MAP. Below is a summary of the main operations in the Log-MAP algorithm.

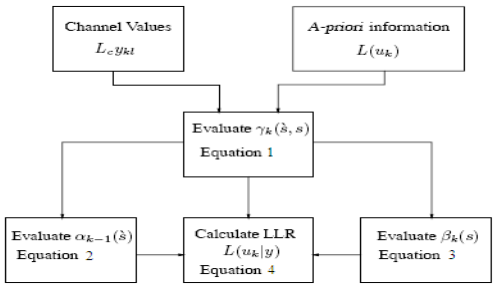

Figure 4. Summary of the key operations in the MAP algorithm.

The equations are as follows:

$$\gamma_k(s',s) = \frac{1}{2}u_k L(u_k) + \frac{Lc}{2}\sum_{l=1}^{n} x_{kl} y_{kl} \qquad \text{(Eq. 1)}$$

$$\alpha_k(s) = \underset{s'}{MAX}{}^*\left(\alpha_{k-1}(s') + \gamma_k(s',s)\right) \quad \text{(Eq. 2)}$$

$$\beta_{k-1}(s') = \underset{s'}{MAX}{}^*\left(\beta_k(s) + \gamma_k(s',s)\right) \quad \text{(Eq. 3)}$$

$$L(u_k \mid \underline{y}) = \underset{\substack{(s',s)=> \\ u_k=+1}}{MAX}{}^*\left(\alpha_{k-1}(s') + \gamma_k(s',s) + \beta_k(s)\right) - \quad \text{(Eq. 4)}$$

$$\underset{\substack{(s',s)=> \\ u_k=-1}}{MAX}{}^*\left(\alpha_{k-1}(s') + \gamma_k(s',s) + \beta_k(s)\right)$$

Observing the equations 2-5, we see one main operator is the called MAX * as described in [7].

IV. Simulations performed

To begin this work first performed in the simulation software turbo code proposed by Berrou, *et al* [1], in order to have a basis with which to compare the results obtained from the simulation.

The result of the simulation is shown in Figure 5, under the conditions given by table 1 which are the same that [2]. The performance show in figure 5 is very similar that the show in [2].

Table 1. Conditions of simulation of turbo code by Berrou.

Modulation	BPSK
Channel	AWGN
Language programming	C, Matlab
Encoder	
Polynomials generators	G1 = 37, G2 = 21
Rate	(R1 = R2 = 2 / 3) R = 1 / 2
Memory	4 (16 states)
Interleaver	non-uniform [5] Length frame N=65536 bits

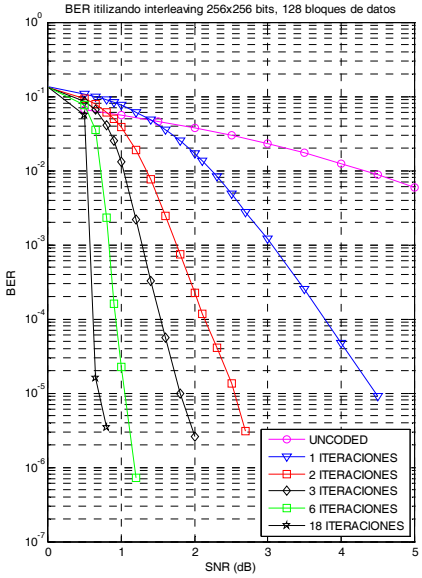

Figure 5. Results of BER of the software simulation of [1].

Subsequently, the simulation in software for the turbo code of 3GPP standard [4]. The conditions were the following:

Table 2. Conditions of simulation of turbo code by 3gpp standard.

Modulation	BPSK
Channel	AWGN
Language programming	C, Matlab
Encoder	
Polynomials generators	G1 = 13, G2 = 15
Rate	R = 1/3
Memory	3 (8 states)
Interleaver	Internal Interleaver specifications given by [4].

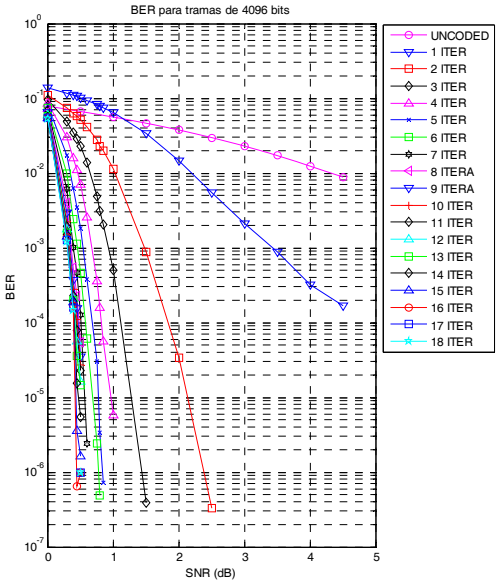

Figure 6. Results of BER of the simulation for N = 4096 3GPP [4].

V. Main Results

Among the activities that are required in this work are the following:

(a) Studying the techniques of normalizing metric because, as we saw in the equations 2-3, these are metric accumulations, so that will help us avoid overflow, [7-9].
(b) Analyze the minimum number of bits, in an actual implementation used fixed-point representation, due to greater use of bits compared to the necessary means greater complexity in the architecture and therefore implies a higher cost, [9-12]. This analysis was reported detailed in [13].
(c) Implementation of the blocks of turbo decoder programmed in VHDL, using the tools of Altera (Quartus II). The figure 7 y 8 shows block diagrams of the general structure of decoder SISO and turbo decoder for N=1024, respectively.
(d) Testing of turbo decoder. This was accomplishing with Model-Sim Altera.

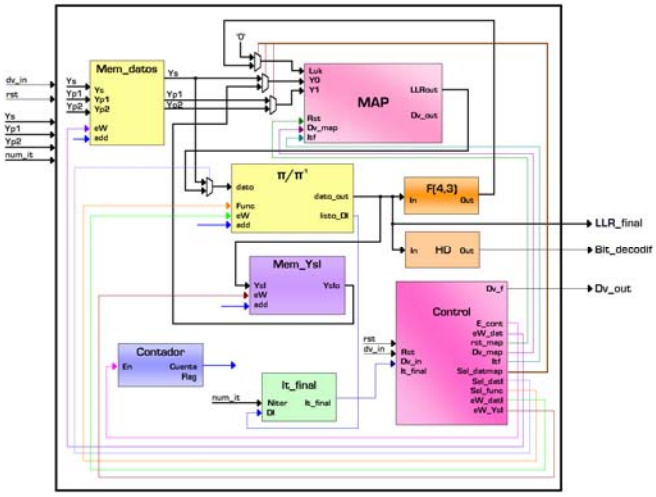

Figure 7. Block diagram of the implementation of turbo decoder, N=1024.

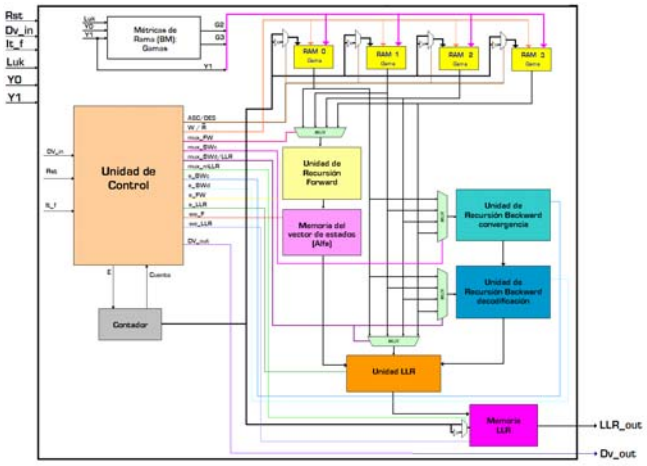

Figure 8. Block diagram of the implementation of decoder SISO, N=1024.

VI. Work to be Done

The activities to be done are:

(a) Validation of turbo decoder.

(b) Get results of turbo code implemented in hardware (Curves probability of error, BER).

(c) Perform comparison of the implementation in hardware and software obtained.

VII. Conclusion

Because of the importance of turbo codes in the field of channel coding, it will suggest an architecture making some improvements to the conventional turbo codes of standard for 3GPP. It has two software simulators that help in the first instance to observe the performance of the turbo code changing some parameters. This work has different aspects (normalization, quantization, and other) that need to be carefully considered when designing and because it requires more analysis.

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